In the component encoder 101A or 101B as shown in Fig. 12B, the reference numeral 111 designates an adder for adding an input bit and outputs of delay elements 112 and 113, each of which delays an input bit until the next bit is supplied; and 114 designates an adder for adding the output of the adder 111 and the output of the delay element 113 to output a parity bit.

Next, the operation of the conventional encoder will be described.

Fig. 13 is a state transition diagram of the component encoders 101A and 101B of Fig. 12B, and Fig. 14 is a trellis diagram of the component encoder 101A or 101B of Fig. 12B. In the following description, it is assumed that the bit length of the information bit sequence D is N, where N is a positive integer, and that D is expressed as $D = \{d_0, d_1, \ldots, d_{N-2}, d_{N-1}\}$.

In the initial state, the delay elements 112 and 113 of the component encoders 101A and 101B are placed at their initial value of zero.

Subsequently, the information bit sequence D is supplied to the component encoder 101A and the interleaver 102. The interleaver 102 rearranges the bits of the information bit sequence D, in which case, the N integers 0, ..., N-1, suffixes of N bits $d_0, \ldots, d_{N-1}$, are rearranged. The mapping of the rearrangement is expressed by "INT" as in Expression (1), and its inverse mapping is expressed by "DEINT". Accordingly, DEINT(INT(k)) = k and INT(DEINT(k)) = k hold.

$$\begin{aligned} &\mathrm{INT}: K \ni k \rightarrow \mathrm{INT}(k) \in K \\ &\mathrm{DEINT}: K \ni k \rightarrow \mathrm{DEINT}(k) \in K \qquad (1) \end{aligned}$$

The information bit sequence D^* ($D^* = \{d^*_k\}$, where $d^*_k = d_{INT(k)}$,

$k = 0, 1, \ldots, N-1$) generated by the interleaver 102 is supplied to the component encoder 101B.

In the component encoder 101A, receiving information bit d_k at a point of time k, the adder 111 calculates the exclusive-OR of the information bit d_k and the bit values held in the delay elements 112 and 113, and supplies its output to the delay element 112 and the adder 114.

Then, the adder 114 calculates the exclusive-OR between the output of the adder 111 and the bit value held in the delay element 113, and outputs the result as the parity bit $p1_k$.

Here, the delay element 112 holds the information bit d_k until the next information bit d_{k+1} is input, and then supplies the information bit d_k to the delay element 113 which holds the one more previous information bit d_{k-1} until the information bit d_k is input.

Likewise, the component encoder 101B receives the information bit d^*_k at the point of time k, and generates and outputs the parity bit $p2_k$.

Thus, at the point of time k, three bits (d_k, $p1_k$, $p2_k$), the information bit, first parity bit and second parity bit, are output simultaneously.

The component encoders 101A and 101B make transitions into new states as shown in Figs. 13 and 14 every time the information bit d_k is input, and the parity bits $p1_k$ and $p2_k$ they generate are determined by their states, that is, by the values held in the delay elements 112 and 113, and by the information bits d_k and d^*_k supplied to the component encoders 101A and 101B.

In the state transition diagram of Fig. 13, a pair of digits in each circle designate the values held in the delay elements 112 and 113 in the component encoder 101A or 101B. For example,

PAGE 3/5 * RCVD AT 2/25/2004 2:27:28 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:7034132220 * DURATION (mm-ss):01-46

two digits "01" express that the delay element 112 holds "0" and the delay element 113 holds "1". On the other hand, a pair of digits affixed to each arrow designate the input information bit d_k and the generated parity bit pi_k (i = 1 or 2). For example, the digits "10" express that the information bit d_k is "1" and the parity bit pi_k is "0".

The trellis of Fig. 14 shows the state transition of the component encoder 101A or 101B along the time sequence. As shown in Fig. 13, each state at the point of time k can make transition to two states at the next point of time k+1, and from two states at the previous point of time k-1. Accordingly, as shown in Fig. 14, the state of the component encoder 101A or 101B makes transition to one of two states in accordance with the information bit and the values held in the delay elements 112 and 113 every time the information bit is input.

In the turbo-code encoder, the component encoders 101A and 101B complete their transition after encoding the final information bit.

Specifically, after the final information bit d_{N-1} is supplied to the component encoder 101A, two additional information bits (d_N, d_{N+1}) are supplied to the component encoder 101A to place its state to "00", that is, to place the contents of the delay elements 112 and 113 to "0". The two additional information bits (d_N, d_{N+1}) are not effective information. In response to the two additional information bits, the component encoder 101A generates two additional parity bits ($p1_N$, $p1_{N+1}$).

Likewise, after supplying the component encoder 101B with the final information bit $d^*_{N-1} = d_{INT(N-1)}$, two additional information bits d^*_N and d^*_{N+1} are supplied thereto so that its state is returned to "00". In response to the two additional

PAGE 4/5 * RCVD AT 2/25/2004 2:27:28 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:7034132220 * DURATION (mm-ss):01-46